WHAT IS CLAIMED IS:

1. A semiconductor structure comprising:

a polysilicon layer;

a barrier layer above the polysilicon layer, the barrier layer comprising tungsten silicide, wherein the barrier layer has substantially etched tungsten oxynitride extrusions formed on the side thereof;

a conductive layer above the barrier layer, the conductive layer comprising titanium silicide, wherein the conductive layer has substantially etched titanium oxynitride extrusions formed on the side thereof; and

a cap above the conductive layer.

2. The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a transistor.

3. The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a synchronous dynamic random access memory array.

4. The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a static memory array.

5. The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a dynamic memory array.

6. The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of an extended data out memory array.

7. The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a wordline in a memory array.

8. The semiconductor structure of Claim 1 wherein the barrier layer is approximately 150 Å thick.

9. The semiconductor structure of Claim 1 wherein the barrier layer has a resistivity of approximately 60 μΩ-cm.

10. The semiconductor structure of Claim 1 wherein the conductive layer is approximately 1000 Å thick.

11. The semiconductor structure of Claim 1 wherein the conductive layer has a resistivity of approximately 15-20 μΩ-cm.

12. The semiconductor structure of Claim 1 wherein the polysilicon layer is above a semiconductor substrate comprising silicon.

13. A semiconductor structure comprising:

a polysilicon layer;

a barrier layer above the polysilicon layer, the barrier layer comprising metal silicide, wherein the barrier layer has substantially etched metal oxynitride extrusions formed on the side thereof;

a conductive layer above the barrier layer, the conductive layer comprising metal silicide, wherein the conductive layer has substantially etched metal oxynitride extrusions formed on the side thereof; and

a cap above the conductive layer.

14. The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a transistor.

15. The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a synchronous dynamic random access memory array.

16. The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a static memory array.

17. The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a dynamic memory array.

18. The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of an extended data out memory array.

19. The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a wordline in a memory array.

20. The semiconductor structure of Claim 13 wherein the barrier layer is approximately 150 Å thick.

21. The semiconductor structure of Claim 13 wherein the barrier layer has a resistivity of approximately 60 $\mu\Omega$-cm.

22. The semiconductor structure of Claim 13 wherein the conductive layer is approximately 1000 Å thick.

23. The semiconductor structure of Claim 13 wherein the conductive layer has a resistivity of approximately 15-20 μΩ-cm.

24. The semiconductor structure of Claim 13 wherein the polysilicon layer is above a semiconductor substrate comprising silicon.

25. A semiconductor stack in a semiconductor device having at least a side comprising a tungsten silicide layer, wherein the tungsten silicide layer has substantially etched tungsten oxynitride extrusions formed on the side thereof.

26. The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a transistor.

27. The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a synchronous dynamic access random memory array.

28. The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a static memory array.

29. The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a dynamic memory array.

30. The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of an extended data out memory array.

31. The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a wordline in a memory array.

32. The semiconductor stack of Claim 25, wherein the tungsten silicide layer is approximately 150 Å thick.

33. The semiconductor stack of Claim 25, wherein the tungsten silicide layer has a resistivity of approximately 60 μΩ-cm.

34. A semiconductor stack in a semiconductor device having at least a side comprising a titanium silicide layer, wherein the titanium silicide layer has substantially etched titanium oxynitride extrusions formed on the side thereof.

35. The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a transistor.

36. The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a synchronous dynamic access random memory array.

37. The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a static memory array.

38. The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a dynamic memory array.

39. The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of an extended data out memory array.

40. The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a wordline in a memory array.

41. The semiconductor stack of Claim 34, wherein the titanium silicide layer is approximately 1000 Å thick.

42. The semiconductor stack of Claim 34,wherein the titanium silicide layer has a resistivity of approximately 15-20 μΩ-cm.

43. A semiconductor stack having at least a side comprising a metal silicide layer, wherein the metal silicide layer has substantially etched metal oxynitride extrusions formed on the side thereof.

44. The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a transistor.

45. The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a synchronous dynamic access random memory array.

46. The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a static memory array.

47. The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a dynamic memory array.

48. The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of an extended data out memory array.

49. The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a wordline in a memory array.